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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO. AUS920000227US1

In re Application of:	§	
	§	
WOLFGANG ROESNER, ET AL.	§	Examiner: **UNKNOWN**
	§	
Serial No.: **09/751,803**	§	
	§	
Filed: **29 DECEMBER 2000**	§	Art Unit: **UNKNOWN**
	§	
For: **SIGNAL OVERRIDE FOR SIMULATION MODELS**	§	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows.

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service, with sufficient postage, as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D. C. 20231.

Date of Deposit: 2/21/2001 **By:** Dena Faris
DENA FARIS

IN THE CLAIMS

Please add claims 5-12 as follows

5. A system for overriding a signal during model simulation, said system comprising:

processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;

processing means for declaring a signal override during model simulation; and

processing means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means.

6. The system of claim 5, wherein said processing means for declaring a signal override further comprises processing means for instantiating an override enable port for delivering an override enable signal.

7. The system of claim 6, further comprising processing means for delivering said override enable signal from said override enable port to said signal selection means.

8. The system of claim 6, further comprising:

processing means for instantiating a latch that stores an override disable bit; and

processing means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection

means.

9. A computer program product for overriding a signal during model simulation, said computer program product comprising:

processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;

instruction means for declaring a signal override during model simulation; and

instruction means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means.

10. The computer program product of claim 9, wherein said instruction means for declaring a signal override further comprises instruction means for instantiating an override enable port for delivering an override enable signal.

11. The computer program product of claim 10, further comprising instruction means for delivering said override enable signal from said override enable port to said signal selection means.

12. The computer program product of claim 10, further comprising:

instruction means for instantiating a latch that stores an override disable bit; and

instruction means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection means.

REMARKS

Figure 8C was included with filing of the Patent Application, as indicated in the specification. However, the figure corresponding to **Figure 8C** was originally mislabeled as **Figure 8B**. Please find attached the amended figures in which **Figures 8, 8A and 8B**, have been re-labeled as **Figures 8A, 8B and 8C**, consistent with the specification.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM Corporation Deposit Account No.09-0465. No extension of time is believed to be necessary. However, in the event an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time to IBM Corporation Deposit Account No.09-0465.

Respectfully submitted,

Matthew W. Baca
Reg. No. 42,277
BRACEWELL & PATTERSON, LLP
Suite 350 Lakewood on the Park
7600B N. Capital of Texas Highway
Austin, Texas 78731
(512) 343-6116

ATTORNEY FOR APPLICANT(S)

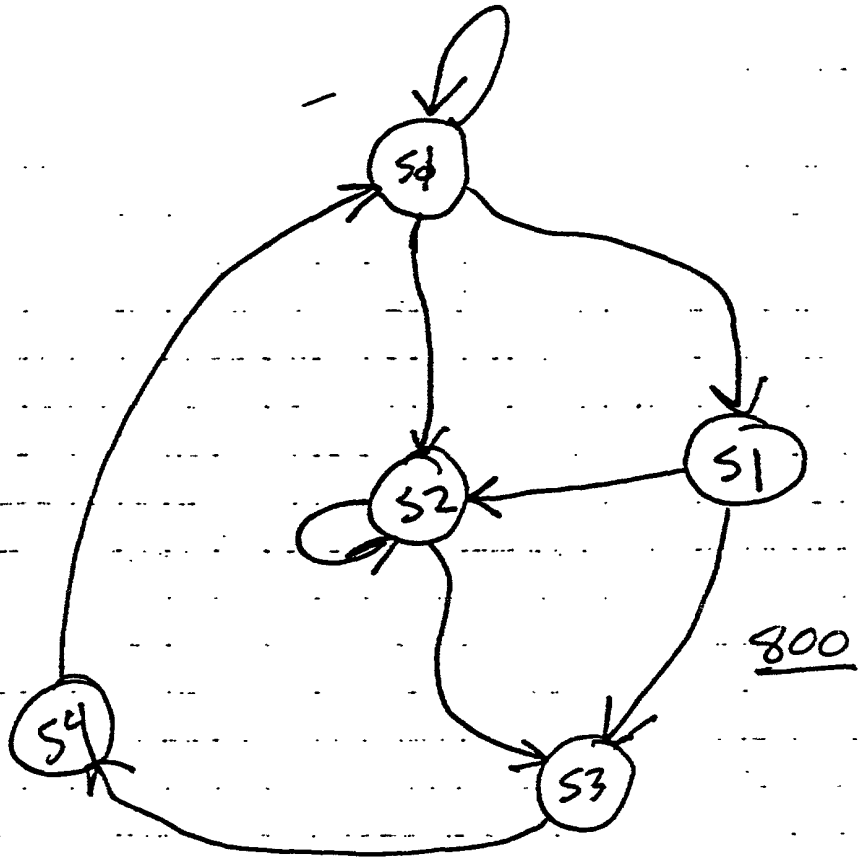

FIG. 8A (Amended)

(Prior Art)

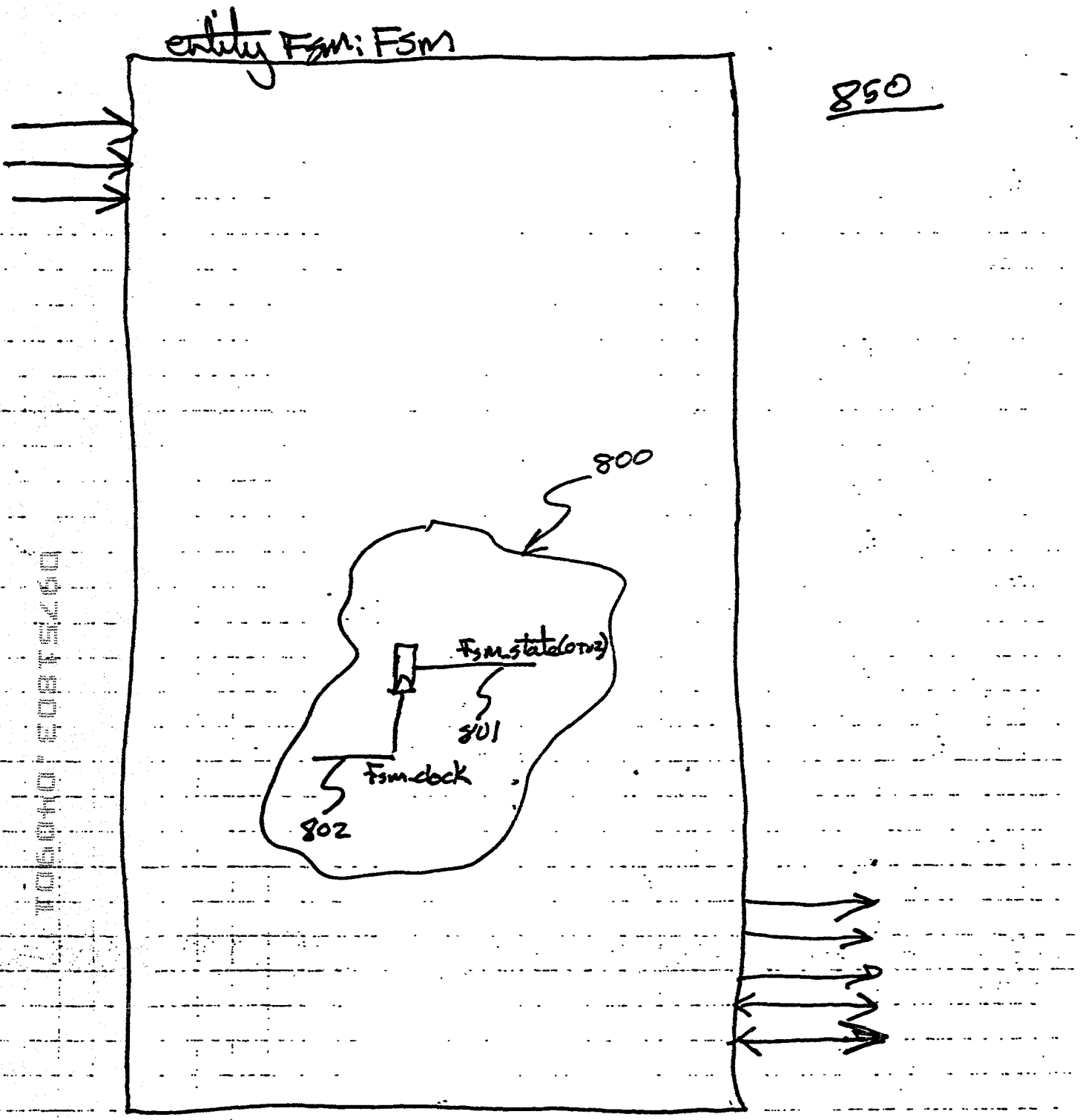

FIG. 8B (Amended)
(Prior Art)

```
entity Fsm IS
  PORT(
        .... ports for entity Fsm ....
  );
ARCHITECTURE Fsm of Fsm IS
BEGIN
        .... HDL code For Fsm and rest of the entity...

        fsm_state(0 to 2) <= ... signal 801 ....

853 {   --!! Embedded Fsm : exampleFsm;
859 {   --!! clock         : (fsm_clock);
854 {   --!! state_vector  : (fsm_state(0 to 2));
855 {   --!! states        : (s0,s1,s2,s3,s4);
856 {   --!! state_encoding : ('000','001','010','011','100');
857 {   --!! arcs          : (s0=>s0, s0=>s1, s0=>s2,
        --!!                 s1=>s2, s1=>s3, s2=>s2,
        --!!                 s2=>s3, s3=>s4, s4=>s0);
858 {   --!! end Fsm;

END;
```

852

8C

FIG. 8C (Amended)